

# 74LVC2G125

Dual bus buffer/line driver; 3-state

Rev. 10 — 11 June 2008

Product data sheet

## 1. General description

The 74LVC2G125 provides a dual non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (pin  $\overline{\text{OE}}$ ). A HIGH-level at pin  $\overline{\text{OE}}$  causes the output to assume a high-impedance OFF-state. Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using  $I_{\text{OFF}}$ . The  $I_{\text{OFF}}$  circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

## 2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- $\pm 24$  mA output drive ( $V_{\text{CC}} = 3.0$  V)
- CMOS low-power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

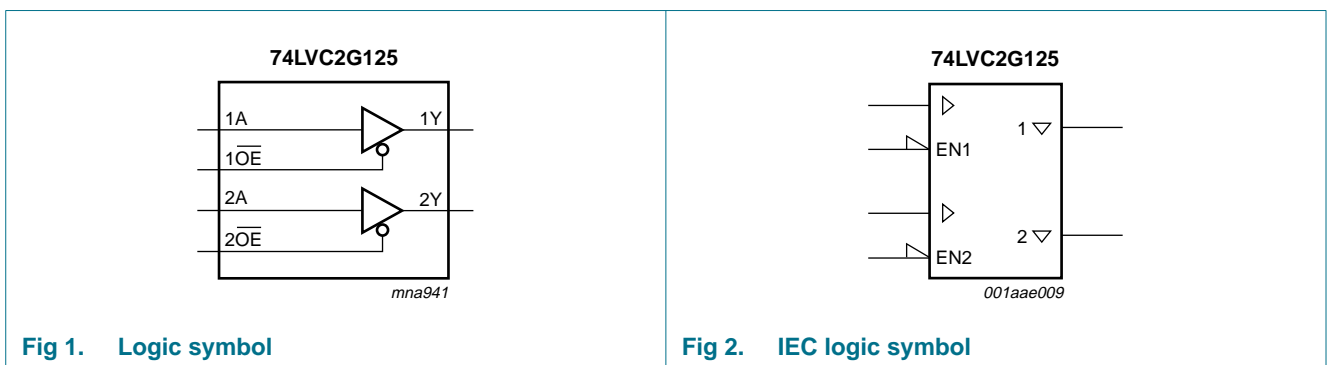
Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G125DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G125DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G125GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC2G125GD	-40 °C to +125 °C	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 × 2 × 0.5 mm	SOT996-2
74LVC2G125GM	-40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm	SOT902-1

### 4. Marking

Table 2. Marking codes

Type number	Marking code
74LVC2G125DP	V25
74LVC2G125DC	V25
74LVC2G125GT	V25
74LVC2G125GD	V25
74LVC2G125GM	V25

### 5. Functional diagram



## 6. Pinning information

### 6.1 Pinning

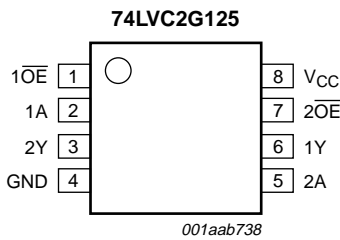


Fig 3. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

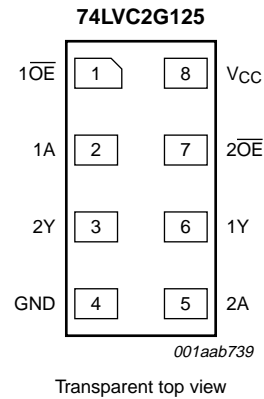


Fig 4. Pin configuration SOT833-1 (XSON8)

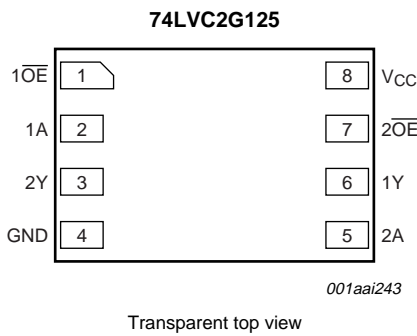


Fig 5. Pin configuration XSON8

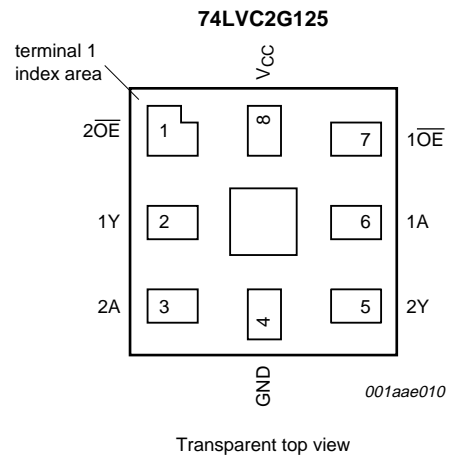


Fig 6. Pin configuration XQFN8U

### 6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT833-1 and SOT996-2	SOT902-1	
1OE, 2OE	1, 7	7, 1	output enable input (active LOW)
1A, 2A	2, 5	6, 3	data input
GND	4	4	ground (0 V)
1Y, 2Y	6, 3	2, 5	data output
VCC	8	8	supply voltage

## 7. Functional description

Table 4. Function table<sup>[1]</sup>

Control	Input	Output
$\overline{\text{nOE}}$	nA	nY
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	Enable mode	[1] -0.5	$V_{CC} + 0.5$	V
		Disable mode	[1] -0.5	+6.5	V
		Power-down mode	[1][2] -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When  $V_{CC} = 0$  V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 package: above 55 °C the value of  $P_{tot}$  derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

For XSON8, XSON8U and XQFN8U packages: above 45 °C the value of  $P_{tot}$  derates linearly with 2.4 mW/K.

## 9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	$V_{CC} = 1.65$ V to 5.5 V; Enable mode	0	$V_{CC}$	V
		$V_{CC} = 1.65$ V to 5.5 V; Disable mode	0	5.5	V
		$V_{CC} = 0$ V; Power-down mode	0	5.5	V

Table 6. Operating conditions ...continued

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	-	10	ns/V

## 10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}[1]$						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3V_{CC}$	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	-	0.45	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	-	0.3	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	-	0.4	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.55	V
		$I_O = 32\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.55	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	-	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.9	-	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	2.2	-	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	2.3	-	-	V
		$I_O = -32\text{ mA}; V_{CC} = 4.5\text{ V}$	3.8	-	-	V
$I_I$	input leakage current	$V_I = 5.5\text{ V or GND}; V_{CC} = 0\text{ V to }5.5\text{ V}$	-	$\pm 0.1$	$\pm 5$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}\text{ or }V_{IL}; V_O = 5.5\text{ V or GND}; V_{CC} = 3.6\text{ V}$	-	$\pm 0.1$	$\pm 10$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I\text{ or }V_O = 5.5\text{ V}; V_{CC} = 0\text{ V}$	-	$\pm 0.1$	$\pm 10$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = 5.5\text{ V or GND}; V_{CC} = 1.65\text{ V to }5.5\text{ V}; I_O = 0\text{ A}$	-	0.1	10	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per pin; $V_I = V_{CC} - 0.6\text{ V}; I_O = 0\text{ A}; V_{CC} = 2.3\text{ V to }5.5\text{ V}$	-	5	500	$\mu\text{A}$
$C_i$	input capacitance		-	2	-	pF

**Table 7. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.70	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.60	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.80	V
		I <sub>O</sub> = 32 mA; V <sub>CC</sub> = 4.5 V	-	-	0.80	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	0.95	-	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.7	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	1.9	-	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.0	-	-	V
		I <sub>O</sub> = -32 mA; V <sub>CC</sub> = 4.5 V	3.4	-	-	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	±20	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V	-	-	±20	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0 V	-	-	±20	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 1.65 V to 5.5 V; I <sub>O</sub> = 0 A	-	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.3 V to 5.5 V	-	-	5	mA

[1] Typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA to nY; see <a href="#">Figure 7</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	3.7	9.1	1.0	11.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	2.5	4.8	0.5	6.0	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.7	4.8	1.0	6.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	2.3	4.3	0.5	5.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.9	3.7	0.5	4.6	ns
t <sub>en</sub>	enable time	nOE to nY; see <a href="#">Figure 8</a> <sup>[3]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	4.3	9.9	1.5	12.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.8	5.6	1.0	7.0	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.3	5.7	1.5	7.1	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	2.4	4.7	0.5	5.9	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	2.0	3.8	0.5	4.8	ns
t <sub>dis</sub>	disable time	nOE to nY; see <a href="#">Figure 8</a> <sup>[4]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	3.5	11.6	1.0	14.1	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	1.8	5.8	0.5	7.6	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.7	4.8	1.0	6.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.7	4.6	1.0	5.9	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.8	3.4	0.5	4.6	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[5]</sup>						
		output enabled	-	18	-	-	-	pF
		output disabled	-	5	-	-	-	pF

[1] Typical values are measured at nominal V<sub>CC</sub> and at T<sub>amb</sub> = 25 °C.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.

[4] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

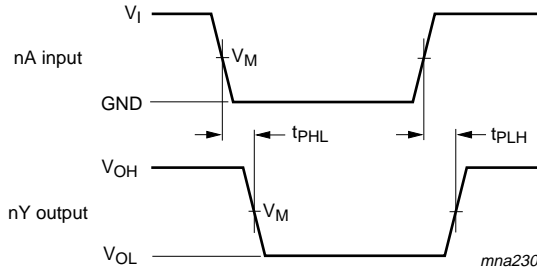
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

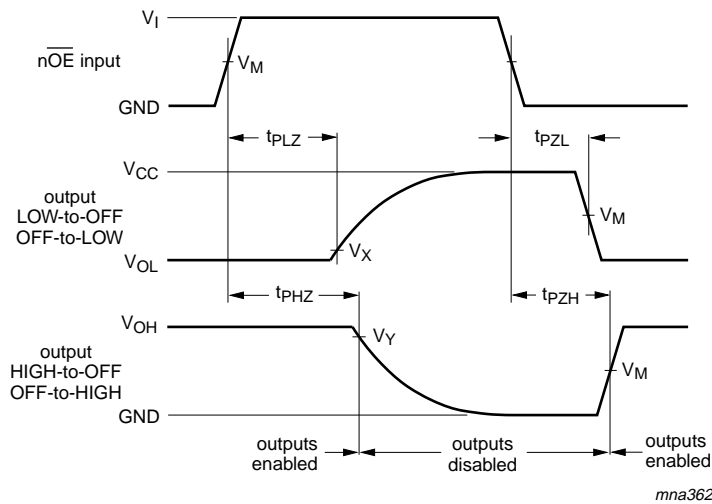
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

12. Waveforms



Measurement points are given in [Table 9](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. Propagation delay input (nA) to output (nY)**



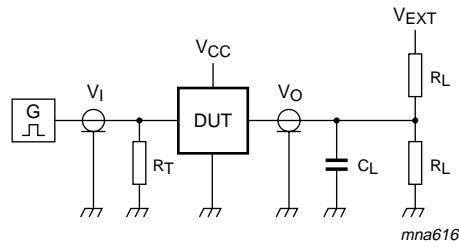
Measurement points are given in [Table 9](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 8. 3-state output enable and disable times**

**Table 9. Measurement points**

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$





Test data is given in [Table 10](#).

Definitions for test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

$V_{EXT}$  = Test voltage for switching times.

**Fig 9. Load circuitry for switching times**

**Table 10. Test data**

Supply voltage $V_{CC}$	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open	GND	$2V_{CC}$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	GND	$2V_{CC}$
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	6 V
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	6 V
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	$2V_{CC}$

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

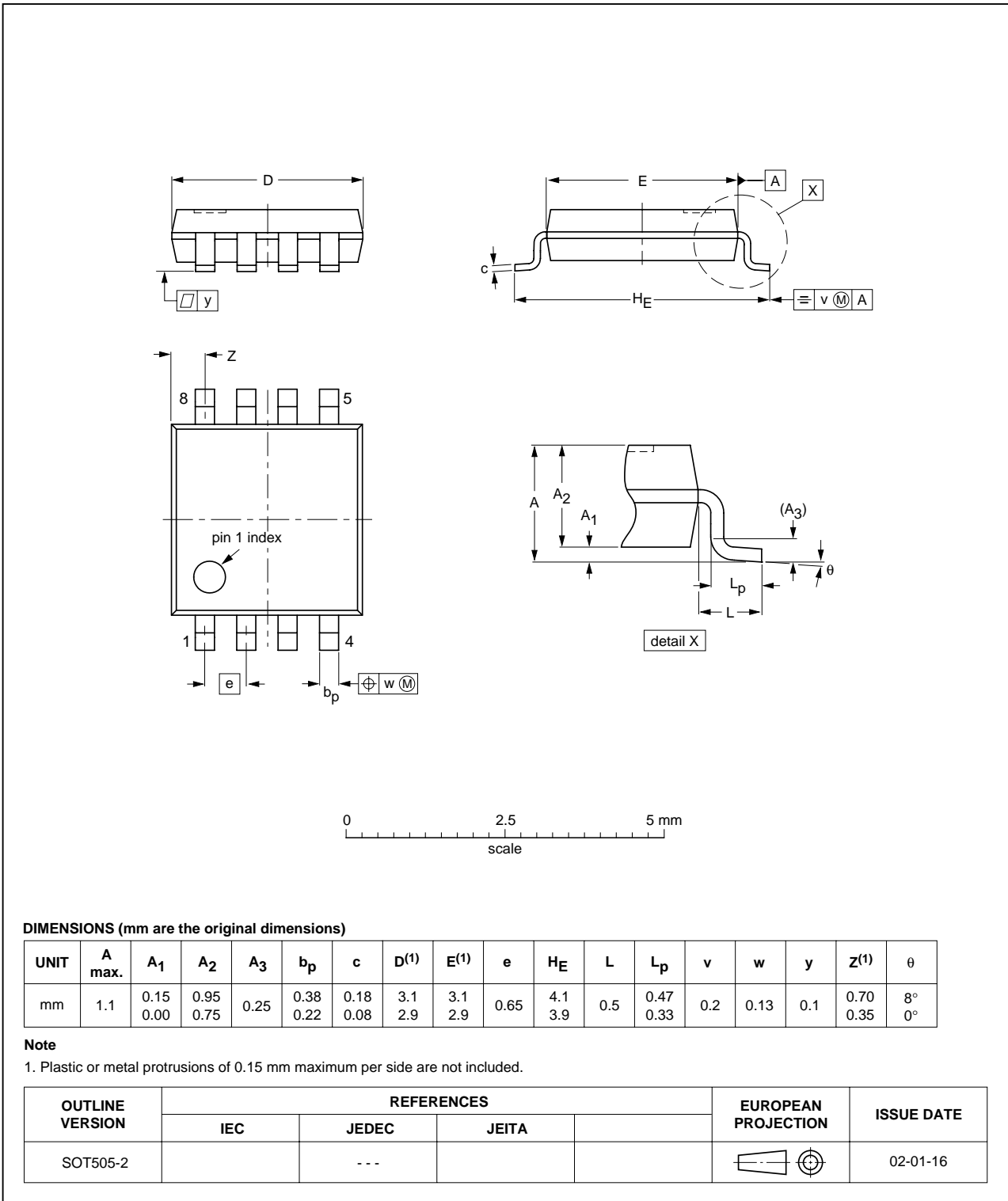


Fig 10. Package outline SOT502-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

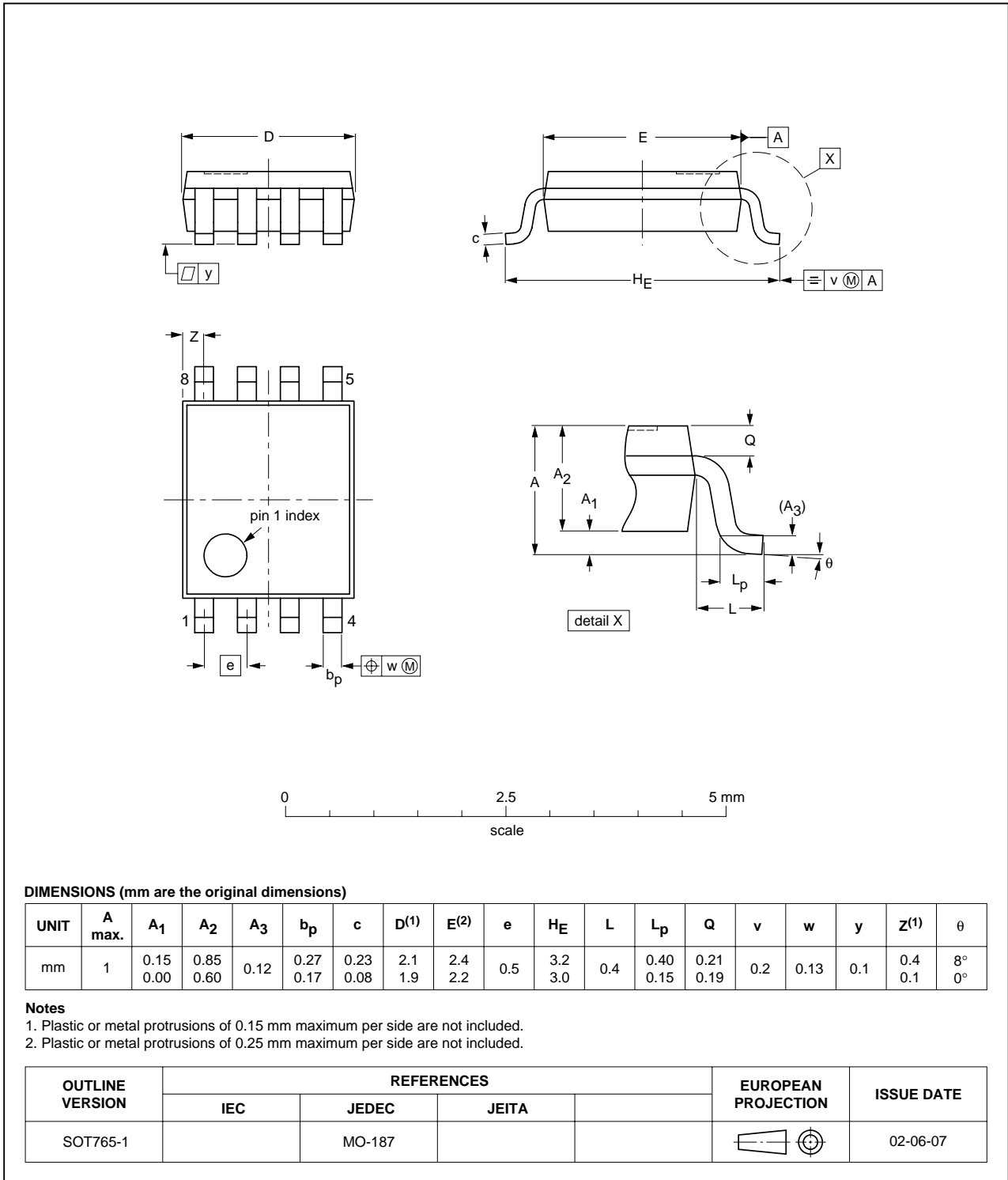


Fig 11. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

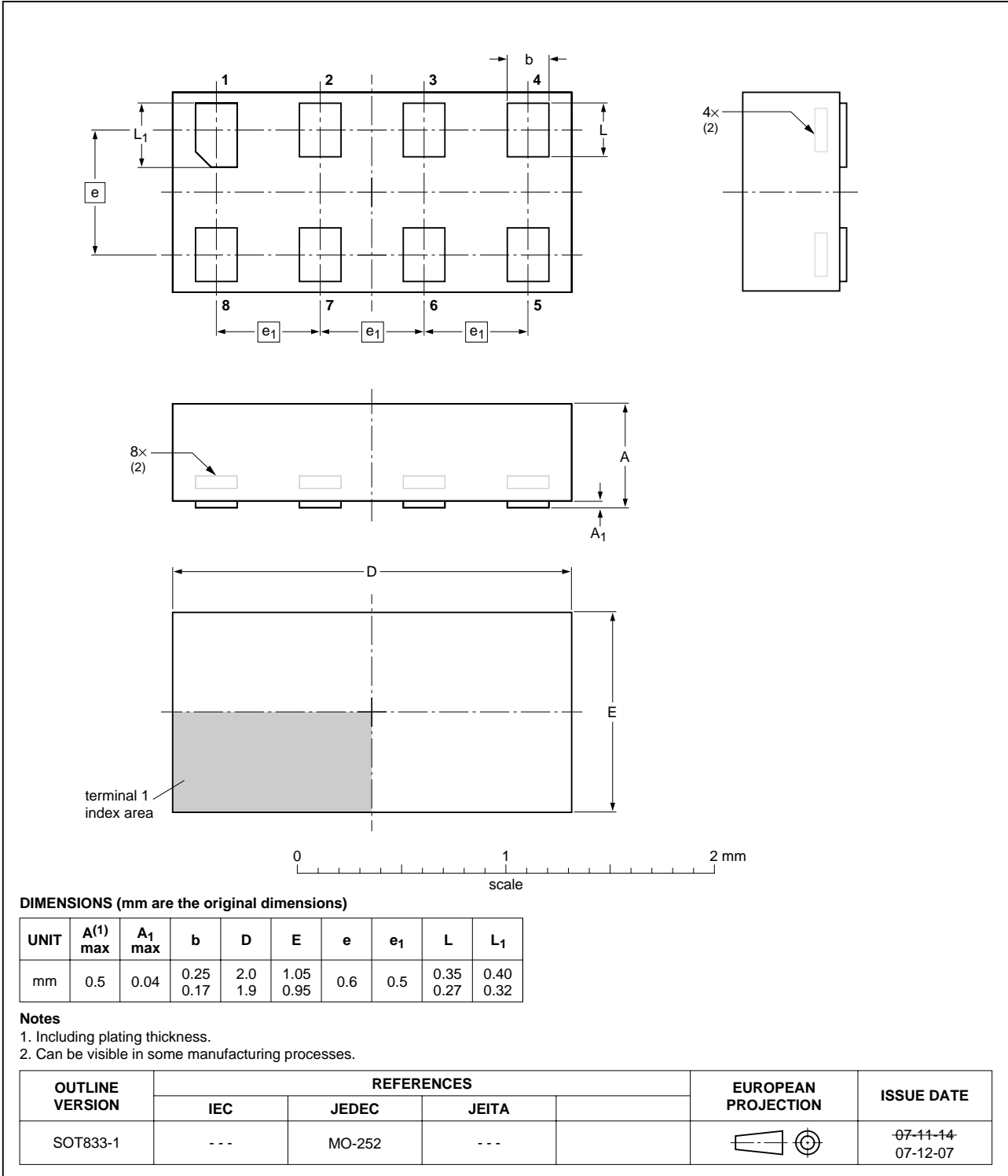


Fig 12. Package outline SOT833-1 (XSON8)

XSON8U: plastic extremely thin small outline package; no leads;  
8 terminals; UTLP based; body 3 x 2 x 0.5 mm

SOT996-2

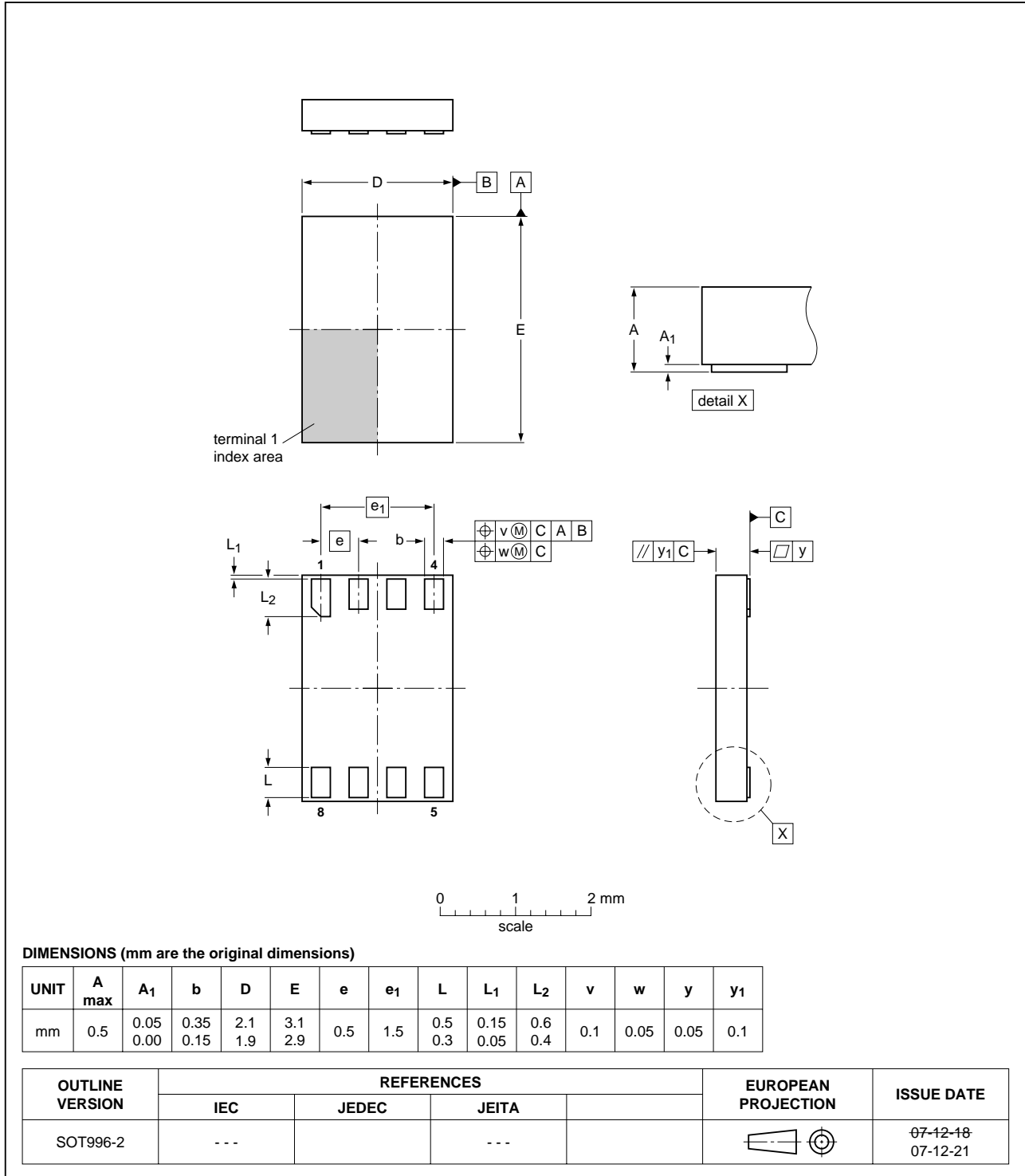


Fig 13. Package outline SOT996-2 (XSON8U)

XQFN8U: plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm

SOT902-1

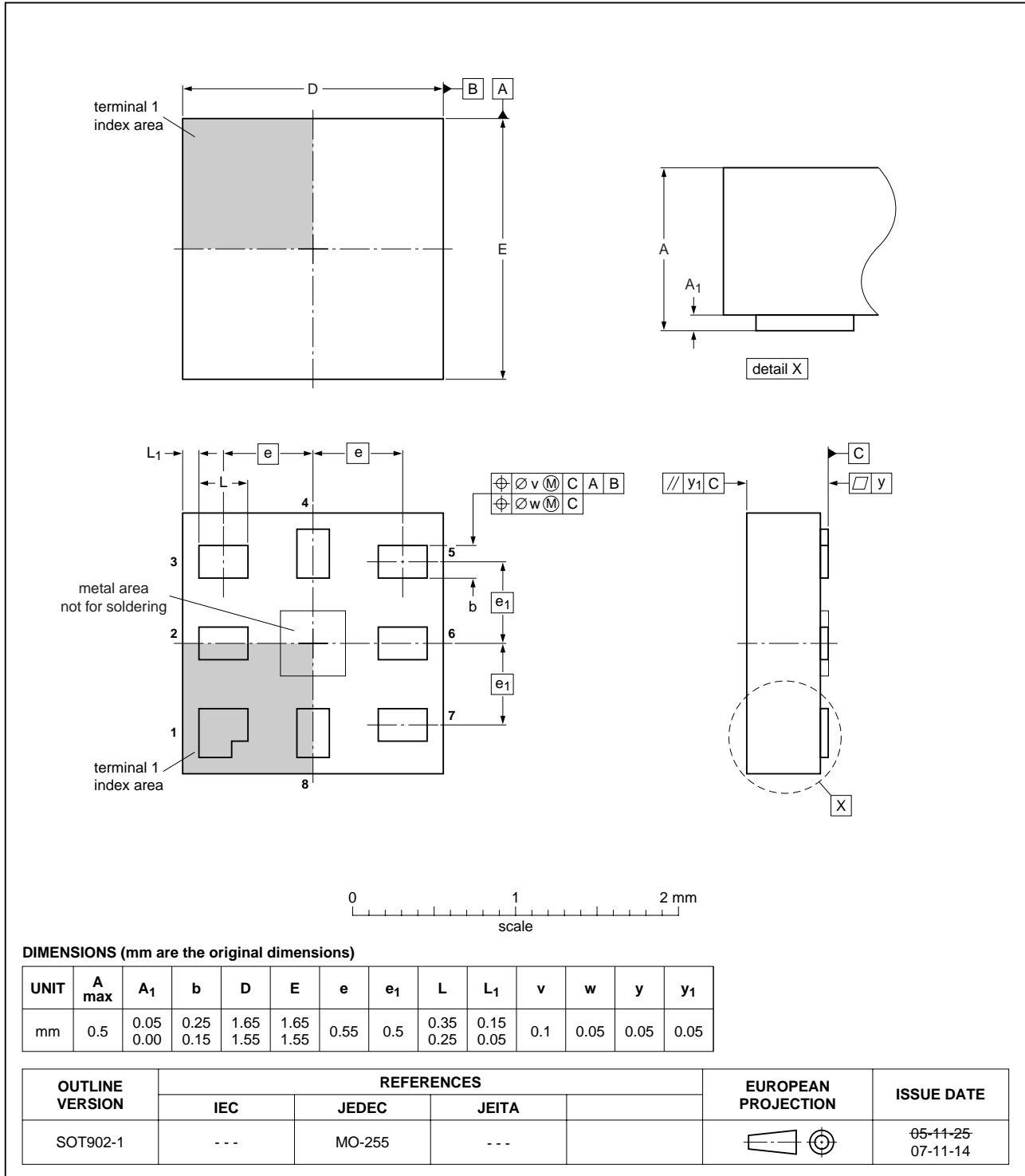


Fig 14. Package outline SOT902-1 (XQFN8U)

## 14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G125_10	20080611	Product data sheet	-	74LVC2G125_9
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 8</a>: derating factor for TSSOP8, VSSOP8, XSON8, XSON8U and XQFN8U package added</li> <li>• Added type number 74LVC2G125GD (XSON8U package)</li> </ul>			
74LVC2G125_9	20080226	Product data sheet	-	74LVC2G125_8
74LVC2G125_8	20070907	Product data sheet	-	74LVC2G125_7
74LVC2G125_7	20060523	Product data sheet	-	74LVC2G125_6
74LVC2G125_6	20051223	Product data sheet	-	74LVC2G125_5
74LVC2G125_5	20050201	Product specification	-	74LVC2G125_4
74LVC2G125_4	20040922	Product specification	-	74LVC2G125_3
74LVC2G125_3	20040109	Product specification	-	74LVC2G125_2
74LVC2G125_2	20030901	Product specification	-	74LVC2G125_1
74LVC2G125_1	20030310	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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